REMARKS

Claims 1-19 were examined and reported in the Office Action. Claims 1-19 are rejected. Claims 1-19 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. In the Drawings

It is asserted in the Office Action that the drawings are objected to because they do not include reference characters 1011 and 1001 as referred to in the specification on page 7, line 25. Applicant notes that reference to registers 1011 and 1001 are not to specific drawings, but to Intel Architecture IA-32. The register names are "1011" and "1001." Applicant has amended the specification to more clearly identify the physical registers as known in IA-32. Approval is respectfully requested.

II. 35 U.S.C. §112, first paragraph

A. It is asserted in the Office Action that claims 1 and 11 are rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement. Applicant has amended claims 1 and 11 to overcome the 35 U.S.C. §112, first paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. §112, first paragraph rejection for claim 1 is respectfully requested.

III. 35 U.S.C. § 103

A. It is asserted in the Office Action that Claims 1-4, 6-10, and 17-18 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 5,966,544 issued to Sager in view of U.S. Patent No. 3,603,934 issued to Heath et al. ("Heath"), and further in view of Hennessy and Patterson, Computer Architecture - A Quantitative Approach, 2ND Edition, 1996 ("Hennessey"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three

basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a] processor comprising: a replay queue to receive a plurality of instructions; an execution unit to execute the plurality of instructions; a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions; a checker coupled to the execution unit to determine whether each instruction of the plurality of instructions has executed successfully, and coupled to the replay queue to dispatch to the replay queue each instruction that has not executed successfully, and a counter to count a number of times an independent instruction has one of executed and replayed, wherein the independent instruction and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the independent instruction is prevented from executing until data required by the independent instruction is available."

Applicant's amended claim 17 contains the limitations of "[a] method comprising: receiving an instruction of a plurality of instructions; placing the instruction in a queue with other instructions of the plurality of instructions; speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies; dispatching one of the plurality of

instructions to an execution unit to be executed; executing the instruction; determining whether the instruction executed successfully; routing the instruction and all associated dependent instructions back to the queue if the instruction did not execute successfully; retiring the instruction if the instruction executed successfully and allowing the instruction's associated dependent instructions to execute, and counting a number of times an instruction has one of executed and replayed, wherein the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Therefore, Applicant's claimed invention provides a correct scheduling of dependent instructions for replay allowing for optimum performance and reduced latency.

Sager discloses a microprocessor having replay architecture for data speculation in executing an instruction. Sager also discloses a checker for validating speculated executed instructions. The technique described in Sager has the purpose of preventing thread deadlock by assigning threads alternating priority using an alternating priority scheme. Namely:

Therefore, it is necessary to have a flexible and dynamic alternating priority scheme in which each thread is alternately given priority for some sufficient period of time in order for it to make progress, which in turn can help the other thread make progress. More specifically, each thread is to be alternately given the priority for some period of time initially. . . . As each thread is being executed, its progress is monitored to determine whether it is being stuck. If a particular thread, for example thread 0, has not made any progress in the period of time during which it has priority, then it will be given priority for a longer duration of time the next time it has priority. (*See* column 9, lines 3-18.) (Emphasis added.)

As indicated by the Examiner, Sager has not taught the above-recited features of Claim 1. Accordingly, the Office Action cites Heath and Hennessy. According to the Office Action:

Heath has taught the general idea of when an instruction is erroneously executed, the instruction will be re-executed a predetermined number of times and when that number is executed, corrective measures have to be taken. See column 2, lines 1-14. Heath has not taught what the corrective measures include. However, Hennessy has taught that it is proper to stall the execution of an instruction until data required by the instruction is available. See page 152-154 of Hennessy. A person of ordinary skill in the art would recognize that by using the idea of Heath, a counter could be implemented in Sager so that a predetermined number of replays are attempted, thereby trying to solve the execution error through re-execution. However, when the predetermined number is exceeded, the re-execution of the erroneous instruction would be suspended so that other instructions, which would possibly execute correctly, would use the system resources instead of the continuously erroneous instruction. . . . As a result, it would be obvious to one of ordinary skill in the art at the time the invention was made to modify Sager to include a counter as taught by Heath which allows for instruction replay a predetermined number of times before requiring corrective measures and to have those corrective by stalling the execution of the instruction until its data is available... (Office Action pg. 6-7, ¶12).

Applicants respectfully traverse the contention cited in the Office Action. In fact, Applicants respectfully submit that preventing thread deadlock by assigning threads alternating priority using an alternating priority scheme as taught by Sager, as well as the above-recited features of Claim 1, lack any similarity to sustain an argument that there is a suggestion or motivation to modify the reference or combine the reference teachings of Sager in view of Heath and Hennessy.

As described within Heath:

> During the execution of any of these steps, it is possible that there may be a malfunction in the system. Malfunctions, or errors, can be either short-lived (transient) or long-lived (solid). A transient error may for example be the result of a sudden fluctuation in the power supply or the result of a mechanical shock. Failure of a component, such as a transistor or diode may result in a solid error. (Heath, column 1, lines 27-34.)

As further described within the passage cited in the Office Action:

> In most systems wherein an attempt is made to re-execute an instruction during the course of which an error has been detected, after a predetermined number of unsuccessful attempts to re-execute the instruction, the error would be classified as solid and the system would signal the operator that corrective action was necessary. (Heath, column 2, lines 8-13.) (Emphasis added.)

Accordingly, Heath describes a system wherein:

> Detection of a malfunction of a functional unit (e.g., a parity error) will cause the system to determine whether one-half of the unit is functioning properly. If one-half of the unit is functioning properly, then the good half of the unit will be used twice processing one-half of the data word each time to produce a correct result. . . . The recursive splitting of the functional unit may be continued to any desired limit, but it will generally be preferable not to use a smaller portion of the functional unit than the smallest portion thereof, which can be checked for errors. (Heath, column 2, lines 51-71.)

Based on the cited passages above, Applicant respectfully submits that the teachings of Heath are strictly limited to actions taken in response to a detected hardware malfunction. As indicated, if the malfunction is solid, corrective action by an operator is required. Accordingly, Applicant respectfully submits that the teachings of Heath are directed to actions to be taken in response to hardware malfunctions.

Conversely, the features of Claim 1 are directed to speculatively executed instructions. Unsuccessful execution of speculative such instructions do not occur due to hardware malfunctions, but instead would occur, for example, when the speculative execution uses invalid data. In such situations, the instruction may be re-executed such that during subsequent execution, the instruction processes valid data. In other words:

> Data speculation may involve speculating that data retrieved from a cache memory is valid. Processing proceeds on the assumption that data retrieved from the cache is good. However, when the data in the cache is invalid, the results of the execution of the speculatively executed instructions are disregarded, and the processor backs up to re-execute the instruction that was executed. Stated another way, data speculation assumes that data in a cache memory are correct, that is, that the cache memory contains the result from those instructions on which the present instruction is dependent. Data speculation may involve speculating that data from the execution of an instruction on which the present instruction is dependent will be stored in a location in cache memory such that the data in the cache memory will be valid by the time the instruction attempts to access the location in cache memory. (*See*, Applicant's specification, page 1, line 35 to page 2, line 9.)

As indicated above, the teachings of Sager are directed to situations where a processing priority between threads is used to indicate which one of the two threads is to have priority if both threads compete for a particular resource in order to make progress. (*See*, Sager, column 10, lines 39-42.) In other words, the above-recited features of Claim 1, as well as the teachings of Sager, do not involve situations regarding failed execution of instructions due to hardware malfunctions, nor the recursive splitting of functional units to identify a properly functioning portion. Accordingly, Applicants respectfully submit that one skilled in the art would not combine the teachings of Sager in view of Heath since there is a complete lack of a suggestion or motivation for one skilled in the art of multi-threaded execution to look to a reference regarding the recursive splitting of functional units to identify a properly functioning portion to execute instructions during detection of hardware malfunctions.

Therefore, Applicants respectfully submit that the Examiner has engaged in an improper hindsight-based analysis to render the above-recited features of Claims 1 and 17 obvious over Sager in view of Heath and Hennessy. According to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in

mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art."

Assuming, arguendo, that the Examiner were allowed to rely on the teachings of Sager in view of Heath and Hennessy, Applicant respectfully submits that the recited combination fails to teach each of the above-recited features of Claim 1. As indicated above, the teachings of Sager are strictly limited to assigning alternating priority of threads to prevent thread deadlock. Hence, Applicant respectfully submits that the entire specification of Sager is devoid of any teachings with regards to re-execution of instructions. In other words, since Sager provides no teachings or suggestions with regards to re-execution of instructions, one skilled in the art would not modify the thread execution technique as taught by Sager in view of in response to hardware malfunction detection, as taught by Heath.

Accordingly, Applicants respectfully submit that one skilled in the art would not modify the thread execution and alternating thread priority as taught by Sager to re-execute instructions a predetermined number of times, as taught by Heath. Neither Sager, Heath, Hennessy, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's claims 1 and 17, as listed above. Since neither Sager, Heath, Hennessy, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's claims 1 and 17, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claims 1 and 17 are not obvious over Sager in view of Heath and Hennessy since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1 and 17, namely claims 2-4 and 6-10, and 18, respectively, would also not be obvious over Sager in view of Heath and Hennessy for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 1-4, 6-10 and 17-18 are respectfully requested.

B. It is asserted in the Office Action that Claims 11-15 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Sager in view of Heath in view of Hennessy, as applied above, and further in view of Johnson, Superscalar Microprocessor Design, 1990 ("Johnson"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's claim 11 contains the limitations of "[a] processor comprising: a replay queue to receive a plurality of instructions; at least two execution units to execute the plurality of instructions; at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies; a counter to count a number of times an independent instruction has one of executed and replayed, and a checker coupled to the execution units to determine whether each instruction has executed successfully, and coupled to the replay queue to communicate each instruction that has not executed successfully, wherein the independent instruction and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the independent instruction is prevented from executing until data required by the independent instruction is available."

Regarding Sager, Heath and Hennessy, the same arguments above with respect to claims 1 and 17 similarly apply to claim 11. Regarding the citing of Johnson in the Office Action, Applicant respectfully submits that the Examiner is prohibited from relying on the combination of Sager in view of Heath since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of Sager in view of Heath and further in view of Johnson.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of Johnson would fail to rectify deficiencies of the combination of Sager in view of Heath and Hennessy to limit execution of the instruction to when the instruction is safe to execute, as recited by Claims 11 ("prevented from executing until data required by the independent instruction is available, once re-execution of the instruction exceeds the maximum number of replays"). Accordingly, Applicant

respectfully submits that Claim 11 is patentable over the combination of Sager in view of Heath, Hennessy and further in view of Johnson, since the combination of references fail to teach or suggest each of the above-recited features of Claim 11.

Accordingly, Applicants respectfully submit that one skilled in the art would not modify the thread execution and alternating thread priority as taught by Sager to re-execute instructions a predetermined number of times, as taught by Heath. Neither Sager, Heath, Hennessy, Johnson, nor the combination of the four, teach, disclose or suggest the limitations contained in Applicant's claim 11, as listed above. Since neither Sager, Heath, Hennessy, Johnson, nor the combination of the four, teach, disclose or suggest all the limitations of Applicant's claim 11, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 11 is not obvious over Sager in view of Heath, Hennessy and further in view of Johnson since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 11, namely claims 12-15, would also not be obvious over Sager in view of Heath, Hennessy and further in view of Johnson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 11-15 are respectfully requested.

C. It is asserted in the Office Action that Claims 1-4, 6, 9-10, and 17-19 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 6,212,626 issued to Merchant et al. ("Merchant"), in view of Heath, and further in view of Hennessy. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Regarding Claims 1 and 17, data required by the independent instruction is available, once re-execution of the instruction exceeds the maximum number of replays.

As indicated above, the teachings of Heath are strictly limited to techniques for executing instructions upon detection of a hardware malfunction by using the recursive splitting of functional units to identify a properly functioning portion. As taught by Heath, when an instruction has been re-executed a predetermined number of times, an

operator is notified. Accordingly, Applicant respectfully submits that the combination of Merchant in view of Heath fails to teach each of the above-recited features of Claims 1 and 17 since neither Claim 1 nor Claim 17 recite the notification of an operator once an instruction has been replayed a maximum number of times.

Furthermore, Applicant respectfully submits that the teachings of Merchant are directed to out-of-order processors, as well as re-execution of instructions, which is not due to hardware malfunctions, but instead may be due to invalid data associated with an instruction due to a cache miss. Accordingly, Applicant respectfully submits that one skilled in the art would not look to the teachings of Heath when dealing with out-of-order processors and speculative execution of instructions, since the teachings of Heath are completely devoid of out-of-order processors and speculative execution of instructions.

Therefore, Applicants respectfully submit that the Office Action has failed to illustrate some suggestion or motivation to combine or modify the reference teachings of Merchant in view of Heath, as suggested by the Office Action. Consequently, the above-recited features of Claims 1 and 17 could only be arrived at through inappropriate hindsight.

Neither Merchant, Heath, Hennessy, nor the combination of the three, teach, disclose or suggest the limitations contained in Applicant's claims 1 and 17, as listed above. Since neither Merchant, Heath, Hennessy, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's claims 1 and 17, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claims 1 and 17 are not obvious over Merchant in view of Heath and Hennessy since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1 and 17, namely claims 2-4 and 6-10, and 18-19, respectively, would also not be obvious over Merchant in view of Heath and Hennessy for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 1-4, 6-10 and 17-18 are respectfully requested.

D. It is asserted in the Office Action that Claims 11-15 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Merchant in view of Heath in view of Hennessy, as applied above, and further in view of Johnson as applied above. Applicant respectfully traverses the aforementioned rejection for the following reasons.

As discussed above, Applicant respectfully submits that the Examiner is prohibited from relying on the combination of Merchant in view of Heath since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of Merchant in view of Heath and Hennessy and further in view of Johnson.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of Johnson would fail to rectify deficiencies of the combination of Merchant in view of Heath to limit execution of the instruction to when a required data for the instruction is available, as recited by Claim 11, once re-execution of the instruction exceeds the maximum number of replays ("prevented from executing until data required by the independent instruction is available, once re-execution of the instruction exceeds the maximum number of replays.").

Neither Merchant, Heath, Hennessy, Johnson, nor the combination of the four, teach, disclose or suggest the limitations contained in Applicant's claim 11, as listed above. Since neither Merchant, Heath, Hennessy, Johnson, nor the combination of the four, teach, disclose or suggest all the limitations of Applicant's claim 11, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 11 is not obvious over Merchant in view of Heath, Hennessy and further in view of Johnson since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claim 11, namely claims 12-15, would also not be obvious over Merchant in view of Heath, Hennessy and further in view of Johnson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 11-15 are respectfully requested.

E. It is asserted in the Office Action that Claims 5 and 19 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Sager in view of Heath in view of Hennessey, as applied above, and further in view of U. S. Patent No. 5,944,818 issued to Baxter et al. ("Baxter"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Regarding the citation of Baxter in the Office Action, Applicant respectfully submits that the Examiner is prohibited from relying on the combination of Sager in view of Heath since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of Sager in view of Heath and Hennessy and further in view of Baxter.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of Baxter would fail to rectify deficiencies of the combination of Sager in view of Heath and Hennessy to limit execution of the instruction to when the instruction is safe to execute, as recited by Claim 1 ("prevented from executing until data required by the independent instruction is available, once re-execution of the instruction exceeds the maximum number of replays") and as recited in Claim 17 "if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Accordingly, Applicants respectfully submit that Claims 1 and 17 are both patentable over the combination of Sager in view of Heath and further in view of Baxter, since the combination of references fail to teach or suggest each of the above-recited features of Claims 1 and 17.

Since neither Sager, Heath, Hennessy, Baxter, nor the combination of the four, teach, disclose or suggest all the limitations of Applicant's claims 1 and 17, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claims 1 and 17 are not obvious over Sager in view of Heath, Hennessy and further in view of Baxter since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 1 and 17, namely claims 5, and 19, respectively, would also not be

obvious over Sager in view of Heath, Hennessy and further in view of Baxter for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 5 and 19 are respectfully requested.

F. It is asserted in the Office Action that Claim 16 is rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Sager in view of Heath in view of Hennessey in view of Johnson, as applied above, and further in view of Baxter, as applied above. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant respectfully submits that the Examiner is prohibited from relying on the combination of Sager in view of Heath and Hennessy since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of Sager in view of Heath and Hennessy and further in view of Baxter and Johnson.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of Baxter and Johnson would fail to rectify deficiencies of the combination of Sager in view of Heath and Hennessy to limit execution of the instruction to when the instruction is safe to execute, as recited by Claim 11 ("prevented from executing until data required by the independent instruction is available, once re-execution of the instruction exceeds the maximum number of replays")

Since neither Sager, Heath, Hennessy, Baxter, Johnson nor the combination of the five, teach, disclose or suggest all the limitations of Applicant's claim 11, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 11 is not obvious over Sager in view of Heath, Hennessy and further in view of Baxter and Johnson since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that indirectly depends from claim 11, namely claim 16, would also not be obvious over Sager in view of Heath, Hennessy and further in view of Baxter and Johnson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection for Claims 16 is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-19 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: September 22, 2004

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on September 22, 2004.

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Jean Svoboda